THE INVENTION CLAIMED IS:

1. A method for controlling the flow of data between a first and second clock domain comprising:

selecting one of a plurality of ports included in a physical layer interface in the second clock domain to which to send data; and

transmitting data from a transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain.

2. The method of claim 1 wherein selecting one of a plurality of ports included in a physical layer interface in the second clock domain to which to send data includes selecting, in the first clock domain, one of a plurality of ports included in a physical layer interface in the second clock domain to which to send data.

3. The method of claim 1 wherein transmitting data from the transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain includes:

transmitting data for the selected port from the transmit buffer to an asynchronous buffer;

transmitting the data from the asynchronous buffer to an internal buffer of a physical layer device included in the physical layer interface, the physical layer device including the selected port; and

transmitting the data from the internal buffer of the physical layer device to the selected port.

4. The method of claim 3 further comprising resetting polling results after a predetermined portion of a data transmission from the asynchronous buffer to the selected

port in the physical layer interface in the second clock domain is complete.

5. The method of claim 1 wherein selecting one of the plurality of ports included in the physical layer interface in the second clock domain to which to send data includes:

polling each of the plurality of ports in the physical layer interface in the second clock domain to determine available ports which may receive data;

sending the polling results to the first clock domain; and

selecting, in the first clock domain, a port from the available ports included in the physical layer interface in the second clock domain to which to send data.

6. The method of claim 5 wherein sending the polling results to the first clock domain includes sending the polling results to the first clock domain after a predetermined portion of a previous data transmission from the transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain is complete.

7. A method for controlling the flow of data from a first clock domain to another clock domain comprising:

selecting one of a plurality of ports included in one of a plurality of physical layer devices included in one of a plurality of physical layer interfaces to which to send data, each of the plurality of physical layer devices operating in the other clock domain;

transmitting data for the selected port from a first buffer operating in the first clock domain to an

asynchronous buffer, the asynchronous buffer corresponding to the one of the plurality of physical layer interfaces;

transmitting the data from the asynchronous buffer to the physical layer device that includes the selected port; and

transmitting the data from the selected port.

8. The method of claim 7 wherein selecting one of a plurality of ports includes selecting one of a plurality of ports to which to send data based on a polling response from one or more of the plurality of ports and based on a previous port of the plurality of ports to which data was transmitted.

9. The method of claim 7 wherein transmitting data for the selected port from a first buffer to an asynchronous buffer includes transmitting data between a synchronous domain and an asynchronous domain.

10. The method of claim 7 wherein transmitting data from the selected port includes:

transmitting data from an internal buffer of one of the plurality of physical layer devices to the selected port, the physical layer device including the selected port; and

transmitting the data from the selected port.

11. The method of claim 7 wherein selecting one of a plurality of ports includes selecting one of a plurality of ports using a round robin algorithm.

12. The method of claim 7 wherein selecting one of a plurality of ports includes selecting one of a plurality of

ports to which to send data based on a polling response from one or more of the plurality of ports.

13. The method of claim 12 wherein the polling response from one or more of the plurality of ports indicates whether one or more of the plurality of ports may receive data.

14. A network processor comprising:

a transmit buffer in a first clock domain;

a physical layer interface, in a second domain, the physical layer interface including a plurality of physical layer devices; and

logic coupled to the transmit buffer and physical layer interface, and adapted to:

select one of a plurality of ports included in the physical layer interface to which to send data; and

transmit data from the transmit buffer to the selected port in the physical layer interface.

15. A network processor comprising:

a transmit buffer in a first clock domain;

a first asynchronous buffer coupled to the transmit buffer;

a first physical layer interface, in a second domain, coupled to the first asynchronous buffer, the first physical layer interface including a plurality of physical layer devices;

a second asynchronous buffer coupled to the transmit buffer;

a second physical layer interface, in a third clock domain, coupled to the second asynchronous buffer, the second physical layer interface including a plurality of physical layer devices; and

logic adapted to:

select one of a plurality of ports included in one of the first and second physical layer interfaces to which to send data; and

transmit data from the transmit buffer to the selected port.

16. An apparatus comprising:

a transmit buffer in a first clock domain;

an asynchronous buffer coupled to the transmit buffer;

a physical layer interface, in a second domain, coupled to the asynchronous buffer, the physical layer interface including a plurality of physical layer devices each having a plurality of ports;

control logic coupled to the asynchronous buffer and the physical layer interface, and adapted to:

poll each of the plurality of ports in the physical layer interface in the second clock domain to determine available ports which may receive data;

send polling results to the first clock domain; and

select logic coupled to the transmit buffer and asynchronous buffer, and adapted to:

select, in the first clock domain, a port from the available ports included in the physical layer interface in the second clock domain to which to send data; and

transmit data from the transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain.

17. The apparatus of claim 16 wherein the control logic is further adapted to send the polling results to the first clock domain after a predetermined portion of a previous data transmission from the transmit buffer to the selected port in the physical layer interface is completed.

18. The apparatus of claim 16 wherein the select logic is further adapted to:

transmit data for the selected port from the transmit buffer to the asynchronous buffer;

transmit the data from the asynchronous buffer to an internal buffer of a physical layer device included in the physical layer interface, the physical layer device including the selected port; and

transmit the data from the internal buffer of the physical layer device to the selected port.

19. The apparatus of claim 18 wherein the control logic is further adapted to reset polling results after a predetermined portion of a data transmission from the asynchronous buffer to the selected port in the physical layer interface is completed.

20. An apparatus comprising:

a transmit buffer in a first clock domain;

an asynchronous buffer coupled to the transmit buffer;

a physical layer interface, in another clock domain, coupled to the asynchronous buffer, the physical layer interface including a plurality of physical layer devices;

logic coupled to the transmit buffer, asynchronous buffer and the physical layer interface, and adapted to:

select one of a plurality of ports included in one of the plurality of physical layer devices included in the physical layer interface to which to send data;

transmit data for the selected port from the transmit buffer to the asynchronous buffer;

transmit the data from the asynchronous buffer to one of the plurality of physical layer devices, the physical layer device including the selected port; and

transmit the data from the selected port.

21. The apparatus of claim 20 wherein the logic is further adapted to select one of the plurality of ports to which to send data based on a polling response from one or more of the plurality of ports.

22. The apparatus of claim 20 wherein the logic is further adapted to transmit data between a synchronous domain and an asynchronous domain.

23. The apparatus of claim 20 wherein the logic is further adapted to select one of the plurality of ports to which to send data based on a polling response from one or more of the plurality of ports and based on a previous port of the plurality of ports from which data was transmitted.

24. The apparatus of claim 23 wherein the polling response from one or more of the plurality of ports indicates whether one or more of the plurality of ports included in the physical layer interface may receive data.

25. The apparatus of claim 20 wherein the logic is further adapted to:

transmit data from an internal buffer of one of the plurality of physical layer devices to the selected port; and

transmit the data from the selected port.

26. The apparatus of claim 25 wherein the logic is further adapted to select one of the plurality of ports using a round robin algorithm.